

Applic. No. 10/623,067
Response Dated February 7, 2005
Responsive to Office Action of October 5, 2004

Remarks:

Reconsideration of the application is respectfully requested.

Claims 1-26 are presently pending in the application. Claims 1, 15, 22, 25, and 26 have been amended.

In item 1 on page 2 of the above-identified Office Action, the Examiner objected to claims 1, 15, 22, and 26 because of informalities. Specifically, the Examiner objected to the use of the Markush format in the preamble of claims 1, 15, 22, and 26. The claims have been amended such that the preambles of claims 1, 15, 22, 25, and 26 no longer have a Markush format.

In item 2 on page 2 of the above-identified Office Action, claims 1-26 have been rejected under 35 U.S.C. § 102 as allegedly being anticipated by Scott et al. (U.S. Patent No. 6,782,515).

Applicants respectfully traverse the above rejections.

The patent to Scott describes a method for identifying and inserting test points in order to improve the testability of integrated circuits.

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In order to achieve high random pattern testability of an integrated circuit, Scott teaches modifying the digital circuit design in a manner such that potential defects in the integrated circuit can be more easily detected.

More specifically, Scott teaches modifying digital circuit designs by inserting test points to improve random pattern testability. Inserting test points means that additional logic and scanable latches are added to the logic circuits. These additional logic or scanable latches provide additional points of control or points of observation during the testing.

Inserting test points (e.g adding additional latches) improves random patterns testability because signal paths that would otherwise be rarely activated by random patterns are more likely to be activated when the test point is inserted.

The purpose of the tests performed by Scott is mainly testing controllability and observability, especially testing logic circuits for "stuck-at-1", "stuck-at-0" or bridging faults.

In order to optimize testability, Scott selects test points with a genetic algorithm. The essence of the teaching of Scott is creating a genetic algorithm that rapidly converges on a test point solution.

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In contrast, the present invention relates to a method of generating test patterns or input signals that are applied to an integrated circuit using an automatic test equipment for the purpose of a functionality test. A functionality test determines whether the integrated circuit meets its specified requirements such as timing requirements, level requirements or other application specific functions. These requirements are generally specified in the product specification of the integrated circuit.

Thus, the method of Scott concerns inserting test points (e.g. adding latches) at critical locations of the integrated circuits wherein these test points are utilized to find physical or structural faults. In contrast, the present inventions concerns a method of generating a set of test patterns or a set of input signals wherein these test patterns or input signals are used to test the functionality of the integrated circuit with an automatic test equipment.

More specifically, Scott discloses determining test point to be added to an integrated circuit. The test point insertion is optimized by using a genetic algorithm.

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A test point (e.g. an additional logical gate) that is added to an integrated circuit is not a test pattern or input signal that is applied to the input of an integrated circuit. Thus Scott does not disclose generating a set of test patterns or input signals that are applied to an integrated circuit by using an automatic test equipment and consequently Scott does not disclose generating a new set of test patterns or new set of input signals by using a genetic algorithm as defined in claims 1, 15, and 22-26 of the instant application.

The objective of Scott, namely optimizing the placement of test points (i.e. physical devices) in an integrated circuit, is entirely different from the objective of the present invention, namely optimizing test patterns or input signals applied to an integrated circuit by an automatic testing equipment. The mere fact that both methods use a genetic algorithm is not sufficient to reject the claims as being anticipated by the teaching of Scott.

It is accordingly believed that the patent to Scott does not teach or suggest the features of claim 1, 15, or 22-26.

Claims 1, 15, and 22-26 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 15.

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In view of the foregoing, reconsideration and allowance of claims 1-26 are solicited.

Petition for extension is herewith made. Please charge the extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of \$120.00 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Manfred Beck
Reg. No. 45,342

Manfred Beck
For Applicant

MB:cgm

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101